· - •	Application No.	Applicant(s)	
Notice of Allowability	10/008,382	KOSS ET AL	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	
The MAILING DATE of this communication appears on the cover sheet with the correspondence address—All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.			
1. This communication is responsive to <u>AMENDMENT filed 1.</u>	<u>/11/2005</u> .		
2. The allowed claim(s) is/are 1-8 and 10-16. Renumbered as	s claims 1-15.		
<ol> <li>Acknowledgment is made of a claim for foreign priority una a)</li></ol>	been received. been received in Application No		ion from the
Applicant has THREE MONTHS FROM THE "MAILING DATE" on noted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.	of this communication to file a reply of ENT of this application.	complying with the rec	uirements
4. A SUBSTITUTE OATH OR DECLARATION must be submit INFORMAL PATENT APPLICATION (PTO-152) which give			OTICE OF
<ol> <li>CORRECTED DRAWINGS ( as "replacement sheets") mus         <ul> <li>(a)  including changes required by the Notice of Draftspers</li> <li>1)  hereto or 2)  to Paper No./Mail Date</li> <li>(b)  including changes required by the attached Examiner's Paper No./Mail Date</li> </ul> </li> <li>Identifying indicia such as the application number (see 37 CFR 1. each sheet. Replacement sheet(s) should be labeled as such in the</li> </ol>	on's Patent Drawing Review (PTO-S Amendment / Comment or in the O 84(c)) should be written on the drawin	ffice action of gs in the front (not the	back) of
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.			
Attachment(s)			
1. Notice of References Cited (PTO-892)	5. Notice of Informal Pa		)-152)
2. Notice of Draftperson's Patent Drawing Review (PTO-948)	<ol> <li>Interview Summary ( Paper No./Mail Date</li> </ol>		
3. Information Disclosure Statements (PTO-1449 or PTO/SB/08 Paper No./Mail Date 10/24/03			
4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	<ul><li>8. ☑ Examiner's Statement</li><li>9. ☐ Other</li></ul>	nt of Reasons for Allo	wance

## **NOTICE OF ALLOWANCE**

This is a Notice of Allowance in response to AMENDMENT filed 1/11/2005.

Claims 1-8 were previously examined. Claim 9 has been cancelled.

Claims 10-16 are new.

Claims 1-8 and 10-16 are allowed. Renumbered as claims 1-15.

## **EXAMINER'S AMENDMENT**

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Morley C. Tobey, Jr. on February 22, 2006.

CLAIM 1 has been substituted with the amended claim as follows:

Claim 1 (Currently Amended):

An electronic circuit for self-test of a random access memory array having a plurality of memory storage cells in a circuit, wherein the storage cells are organized into a plurality of slice arrays, comprising:

a control circuit, wherein the control circuit is embedded in a control and address block of the RAM circuit;

an address selection circuit, wherein the control circuit directs the address selection circuit to index through memory addresses;

one input/output circuit each associated with each slice array, wherein the control circuit directs each input/output circuit to write data into its associated slice array at an indexed memory address, to read data from the associated slice array at the indexed memory address, and to compare the data read from the associated slice array with that written into the associated slice array at the indexed memory address; and

an error detection circuit, wherein the error detection circuit collects results of self-test data comparisons from each input/output circuit and notifies the control circuit of the results of the self-test data comparisons, wherein:

when a defect is present in one of the slice arrays, the input/output circuit associated with the defective slice array redirects data intended for storage in the defective slice array to an adjacent slice array, and wherein:

when a defect is present in one of the slice arrays, the input/output circuit associated with the defective slice array redirects data read from the adjacent slice array of the defective slice array to the output of the defective slice array.

## **REASONS FOR ALLOWANCE**

The following is an examiner's statement of reasons for allowance:

The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention recited in the independent claim 1, as currently amended, including inter alia, "when a defect is present in one of the slice

arrays, the input/output circuit associated with the defective slice array redirects data intended for storage in the defective slice array to an adjacent slice array, and wherein, when a defect is present in one of the slice arrays, the input/output circuit associated with the defective slice array redirects data read from the adjacent slice array of the defective slice array to the output of the defective slice array".

Claims 2-4, 10 are directly depended upon claim 1, and therefore are also allowable.

Claims 5-8, previously objected to for having allowable subject matter as being dependent upon a rejected base claim, have been rewritten in independent form, as claims 5 and 7, including all of the limitations of the base claim. The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention as recited in claims 5 and 7.

Claims 6-8, 11-16 are directly depended upon claims 5 and 7, and therefore are also allowable.

Consequently, Claims 1-8 and 10-16 are allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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## Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. Patent and Trademark Office Randolph Bldg, 401 Dulany Street, Alexandria, VA 22314 Tel: (571) 272-3824, Fax: (571) 273-3824 james.kerveros@uspto.gov

Date: 23 February 2006 Office Action: Allowance JAMES C KERVEROS

Examiner Art Unit 21/38

By:

ALBERT DECADY

STREETVISORY PATENT EXAMINER

EHVISON'S PATENTER \$100